Japanese Patent Laid-Open No.: Hei 6-61499

Laid-Open Date : March 4, 1994

Application No. : Hei 4-214025

Application Date : August 11, 1992

Applicant : Mitsubishi Electric Corp.

2-2-3, Marunouchi, Chiyoda-ku, Tokyo

Inventor : Hiroshi Onoda

c/o LSI Laboratory K.K., Mitsubishi Electric

4-1, Mizuhara, Itami-shi, Hyogo-ken

Inventor : Atsushi Fukumoto

c/o LSI Laboratory K.K., Mitsubishi Electric

4-1, Mizuhara, Itami-shi, Hyogo-ken

Agent : Hisao Fukami, Attorney (and three others)

[Title of the Invention]

Method of manufacturing a nonvolatile semiconductor memory device

[Abstract]

[Purpose]

To facilitate control for the thickness of a dielectric film between a control gate and a floating gate thereby improving the distribution accuracy of a threshold value voltage

between memory cells.

[Constitution]

In a step of forming a first silicon oxide film 35, a silicon nitride film 37, and a second silicon oxide film 42 successively over a control gate, at least one gate oxidation step for transistors in a peripheral region after forming the silicon nitride film 37 and before forming the second silicon oxide film 42 is provided. Further, this decreases the number of times of fluoric acid treatment as a pretreatment to the gate oxidation conducted after formation of the second silicon oxide film, and scattering for the thickness of the second silicon oxide film 42 attributable to the fluoric acid treatment is decreased.

39, 41: silicon oxide film

42: HTO film

[Scope of the claim for Patent]

[Claim 1]

A method of manufacturing a nonvolatile semiconductor memory device having a memory cell region and a peripheral circuit region comprising:

a step of forming an insulative film on a main surface of a semiconductor substrate;

a step of forming a floating gate on the insulative film;

a step of forming a dielectric film formed by successively stacking a first silicon oxide film, a silicon nitride film and a second silicon oxide film over the floating gate, and

a step of forming a control gate over the dielectric film, in which

the step of forming the dielectric film includes:

a step of successively forming the first silicon oxide film and the silicon nitride film; and

a step of forming the second silicon oxide film on the silicon nitride film after the gate oxidation step at least once, for forming the gate oxide film of transistors in the peripheral circuit region.

[Detailed Description of the Invention]

[0001]

[Industrial Field of Use]

The present invention generally concerns a nonvolatile semiconductor memory device capable of electrically writing and erasing, and a manufacturing method thereof and, more specifically, it relates a structure of a flash memory and a method of manufacturing the same.

[0002]

[Prior Art]

A flash memory is present as a memory device capable of freely writing data and capable of electrically erasing the same. EEPROM constituted with one transistor and capable of electrically erasing written information charges collectively, that is, a so-called flash memory is proposed in USP No. 4,868,619 or "An In-System Reprogrammable 32K×8 CMOS Flash Memory" by Virgil Niles Kynett, et al., IEEE Journal of Solid-State Circuits, vol. 23, No. 5, October 1988.

[0003]

Fig. 12 is a block diagram showing a general constitution of a flash memory. In the drawing, the flash memory comprises a memory cell matrix 100 arranged in a row and column form, an X-address decoder 200, a Y-gate 300, a Y-address decoder 400, an address buffer 500, a writing circuit 600, a sense amplifier 700, input/output buffer 800 and a control logic 900.

[0004]

The memory cell matrix 100 has plural memory transistors arranged in a matrix at the inside thereof. The X-address recorder 200 and the Y-gate 300 are connected for selecting rows and columns of the memory cell matrix 100. The Y-address decoder 400 for giving a selection information for the columns is connected to the Y-gate 300. The address buffer 500 for temporarily storing address information is connected to the X-address decoder 200 and the Y-address decoder 400, respectively.

[0005]

The Y-gate 300 is connected with the writing circuit 600 for conducting writing operation upon data input and the sense amplifier 700 for judging "0" and "1" according to the value of a current flowing upon data output are connected with the Y-gate 300. The input/output buffer 800 for temporarily storing input/output data is connected to the writing circuit 600 and the sense amplifier 700 respectively. The control logic 900 is connected to the address buffer 500 and the input/output buffer 800 for controlling the operation of the flash memory. The control logic 900 conducts control based on a chip enable signal, an output enable signal and a program signal.

[0006]

Fig. 13 is an equivalent circuit diagram showing the outlined constitution of the memory matrix 100 shown in Fig. 12. In the drawing, plural word lines WL_1, WL_2, ..., WL_i extending in the direction of the row and plural bit lines BL_1, BL_2, ..., BL_j extending in the direction of the column are arranged so as to

perpendicular with each other to constitute a matrix. At the intersections for the respective word lines and the respective bit lines are arranged memory transistors Q_{11}, Q_{12}, ... Q_{ij} each having a floating gate. Each drain for each of the memory transistors is connected with each bit line. The control gate of the memory transistor is connected to each word line. The source for the memory transistor is connected with each of source lines S_1, S_2, ... Sources for the memory transistors belonging to an identical row are connected with each other as shown in Fig. 13.

[0007]

Fig. 14 is a fragmentary cross sectional view showing the cross sectional structure of a memory transistor constituting the flash memory described above. The transistor of the flash memory shown in Fig. 14 is referred to as a stack gate type. Fig. 15(a) is an outlined plan view showing a planar arrangement of existent stack gate type flash memory. Fig. 15(b) is a fragmentary cross sectional view taken along line A-A in Fig. 15(a). The structure of the existent flash memory is to be described with reference to the drawings.

[0008]

Referring to Fig. 14 and Fig. 16, an n-type impurity region, for example, an n^+-drain region 84 and an n^+-source region 85 are formed being spaced apart on the main surface of a p-type impurity region 33 disposed over a silicon substrate. A control gate 86 and a floating gate 87 are formed in a region

put between the n^+-drain region 84 and the n^+-source region 85 so as to form a channel region. The floating gate 87 is formed by way of a thin gate oxide film 90 of about 100 Å thickness on the p-type impurity region 83. The control gate 86 is formed by way of an interlayer insulative film 88 over the floating gate 87 so as to be separated electrically from the floating gate 87. The floating gate 87 is formed of a polycrystal silicon layer . The control gate 86 is formed of a polycrystal silicon layer or a stacked film of a polycrystal silicon layer and a high melting metal. An oxide film 89 is formed by depositing to the surface of the silicon substrate 1 and the polycrystal silicon layer constituting the floating gate 87 and the control gate 86 by a CVD method. Further, a smooth coat film 95 is formed so as to cover the floating gate 87 and the control gate 86.

[0009]

As shown in Fig. 15(a), control gates 86 are connected to each other and formed as a word line so as to extend laterally (in the direction of row). Bit lines 91 are arranged so as to intersect the word lines 86 and connect n^+-drain regions 84 arranged in the longitudinal direction (direction of column) to each other. The bit line 91 is electrically connected to each n^+-drain region 84 through a drain contact 96. As shown in Fig. 15(b), the bit line 91 is formed on a smooth coat film 95. As shown in Fig. 15(b), the n^+-source region 85 extends along the extending direction of the word line 86 and is formed in a region surrounded with the word line 86 and a field oxide film

92. Each n^+-drain region 84 is formed also in a region surrounded with the word line 86 and the field oxide film 92.

[0010]

The operation of the flash memory having thus been constituted is to be described with reference to Fig. 14.

[0011]

At first, in the writing operation, a voltage V_D at about 5 to 8 V is applied to the n^+-drain region 84 and a voltage V_G at about 10 to 15 V is applied to the control gate 86. Then, the n^+-source region 85 and the p-type impurity region 83 are kept at a ground potential. In this case, a current of several hundreds μA flows to the channel of the memory transistor. Among electrons flowing from the source to the drain, those electrons accelerated near the drain are formed as electrons having high energy so-called channel hot electrons at the vicinity thereof. The electrons are injected to the floating gate 87 by an electric field generated by the voltage V_G applied to the control gate 86 as shown by an arrow ①. In this way, electrons are accumulated in the floating gate 87 to increase the threshold voltage V_{th} of the memory transistor. The state in which the threshold voltage V_{th} is made higher than a predetermined value is referred to as a written state "0".

[0012]

Then, in the erasing operation, a voltage V_S at about 9 to 12 V is applied to the n^+-source region 85, and the control gate 86 and the p-type impurity region 83 are kept at a ground

potential. Then, the n^+-drain region 84 is opened. Electrons in the floating gate 87 pass the thin gate oxide film 90 due to the tunnel phenomenon under the electric field formed by the voltage V_S applied to the n^+-source region 85 as shown by arrow ②. In this way, the threshold voltage V_{th} of the memory transistor is lowered by the extraction of the electrons in the floating gate 87. The state in which the threshold voltage V_{th} is lower than a predetermined value is referred to as an erased state "1". Since the source for each memory transistor is connected as shown in Fig. 13, all memory cells can be erased collectively by the erasing operation.

[0013]

Further, in the reading operation, a voltage V_G' at about 5 V is applied to the control gate 86 and a voltage V_D' at about 1 V is applied to the n^+-drain region 84. In this case, judgement for "1" or "0" described above is conducted depending on whether the current flows in the channel region of the memory transistor or not, that is, depending on whether the memory transistor is in the ON or OFF state.

[0014]

An existent method of manufacturing a flash memory is to be described with reference to Fig. 16 to Fig. 36. The left part of the drawing depicts a peripheral region and the right part thereof depicts a memory cell region.

[0015]

As shown in Fig. 16, a silicon oxide film 3 of 300 Å

thickness is formed on the main surface of p-type <100> silicon substrate. Then, a silicon nitride film 5 of 500 Å thickness is formed on the silicon oxide film 3 by a CVD (Chemical Vapor Deposition) method. Then, resist 7 is formed on the silicon nitride film 5 and the silicon nitride film 5 over a region to form an n-well is removed by usual photolithography. Then, phosphorus is ion implanted into the silicon substrate 1 using the resist 7 as a mask, under the condition at 60 keV and $1.0 \times 10^{13}/cm^2$. The resist 7 is removed and an oxide film 9 of 5000 Å thickness shown in Fig. 17 is formed by using the silicon nitride film 5 as a mask. Then, the silicon nitride film 5 is removed. Subsequently, boron is ion implanted over a region to form a p-well by using the oxide film 9 as a mask under the condition at 100 keV and $1.0 \times 10^{13}/cm^2$. Fig. 17 shows this state.

[0016]

Then, as shown in Fig. 18, the impurities injected into the silicon substrate 1 are diffused to form an n-well 11 and a p-well 13 under the condition at 1200°C for 6 hours. Then, the field oxide film 9 is removed.

[0017]

As shown in Fig. 19, a silicon oxide film 15 of 300 Å thickness, a polycrystal silicon film of 17 of 1000 Å thickness, a silicon nitride film 19 of 2000 Å thickness and a resist 21 are formed successively above the main surface of the silicon substrate 1. Then, the silicon nitride film 19 over a region to

form a field oxide film is selectively removed by using usual photolithography.

[0018]

As shown in Fig. 20, a resist 23 is formed above the main surface of the silicon substrate 1 and a predetermined pattering is applied to the resist 23. Then, boron is ion implanted into a region to form the field oxide film of the p-well 13 by using the resist 23 as a mask under the condition at 80 keV and $2.5 \times 10^{13}/cm^2$.

[0019]

The resist 21 and the resist 23 are removed and a field oxide film 27 of 7000 Å thickness is formed by using the silicon nitride film 19 as a mask. In this case, a p^+-channel stopper 25 is also formed simultaneously. Then, the silicon nitride film 19 and the polycrystal silicon film 17 are removed to form a state shown in Fig. 21. The p^+-channel channel stopper 25 is not illustrated hereinafter. Then, a resist (not illustrated) is formed above the entire main surface of the silicon substrate 1 shown in Fig. 21 and the resist is removed only for the memory cell region. Then, boron is ion implanted for the control of the threshold voltage of the memory cell by using the resist as a mask.

[0020]

As shown in Fig. 22, the silicon oxide film 15 is removed, and a silicon oxide film 29 of 100 Å thickness is formed above the entire main surface of the silicon substrate 1 by using a

thermal oxidation method. A polycrystal silicon film 31 of about 1000 Å thickness is formed on the entire surface of the silicon oxide film 29 by using a CVD method. The polycrystal silicon film 31 constitutes the floating gate. A resist 33 is formed on the entire surface of the polycrystal silicon film 31 and the resist 33 at the peripheral region is removed.

[0021]

The polycrystal silicon film 31 is removed by etching using the resist 33 as a mask to form a state shown in Fig. 23. Fig. 24 is a cross sectional view in which the memory cell region shown in Fig. 23 is cut along the direction B.

[0022]

Then, as shown in Fig. 25, a silicon oxide film (hereinafter referred to as "HTO" in order to distinguish from thermal oxide film) 35 of about 100 Å thickness is formed above the entire main surface of the silicon substrate 1 by high temperature deposition of an oxide film (hereinafter referred to as "HTO". HTO is an abbreviation of High Temperature Oxide) by using a CVD method. A silicon nitride film 37 of about 100 Å thickness is formed on the HTO film 35 by using a CVD method. Then, an HTO film 42 of about 100 Å thickness is formed on the silicon nitride film 37 by a CVD method. Then, the HTO film 42 and the silicon nitride film 37 are removed selectively by a resist process and, impurities are implanted for controlling the threshold voltage of the transistors in the peripheral region.

[0023]

Then, after removing the HTO film 35 and the silicon oxide film 29 only from the peripheral region, silicon oxide films 39, 41 are formed by a thermal oxidation method to form a cross sectional structure shown in Fig. 26. In Fig. 26, (a) shows the memory region on the right and the n-well 11 and the p-well 13 forming 5 V type transistor on the left, whereas (b) shows an n-well 111 and a p-well 113 forming a high voltage withstanding transistor in the peripheral region.

[0024]

Then, as shown in Fig. 27, only the n-well 111 and the p-well 113 forming the high voltage withstanding transistor in the memory cell region and the peripheral region are covered with a resist film 101, and the silicon oxide film 41 of the n-well 11 and the p-well 13 forming the 5 V type transistor are removed. Subsequently, thermal oxidation for forming the gate oxide film is applied again to form a silicon oxide film 41 of about 150 Å thickness on the surface of the n-well 11 and the p-well 13. In this case, the surface of the n-well 111 and the p-well 113 are thermally oxidized simultaneously to increase the thickness of the silicon oxide film 39 to about 300 Å.

[0025]

As shown in Fig. 29, a polycrystal silicon film 43 of 2500 Å thickness is formed over the silicon oxide film 41 and the HTO film 42 by using a CVD method. The polycrystal silicon film 43 constitutes a control gate in the memory cell region and constitutes a gate electrode in the peripheral region. A resist

45 is formed on the polycrystal silicon film 43 and a predetermined patterning is applied to the resist 45. The polycrystal silicon film 43 is removed by etching using the resist 45 as a mask to form a gate electrode 47 (refer to Fig. 30) and then the resist 45 is removed to form a structure shown in Fig. 30.

[0026]

As shown in Fig. 31, a resist 53 is formed above the entire main surface of the silicon substrate 1. A predetermined patterning is applied to the resist 53 to remove the polycrystal silicon film 43, the HTO film 42, the silicon nitride film 37, the HTO film 35, and the polycrystal silicon film 31 in the memory cell by etching region. The polycrystal silicon film 43 is hereinafter referred to as a control gate 51 and the polycrystal silicon film 31 is referred to as a floating gate 49. Fig. 32 is a cross sectional view for a state in which the memory cell region shown in Fig. 31 is cut along the direction C.

[0027]

The resist 53 shown in Fig. 31 is removed to form a side wall insulative film 55, a source region and a drain region 57 for the memory cell region, a source region and a drain region 59 for the peripheral region, a silicon oxide film 61, a silicon nitride film 62 and a smooth coat film 63 as shown in Fig. 33.

[0028]

A contact hole 66 is formed to the smooth coat film 63, the silicon nitride film 62, the silicon oxide film 61, the

silicon oxide film 29, and the silicon oxide film 41 shown in Fig. 33. An aluminum wiring film 65 is formed by sputtering on the smooth coat film 63 and the aluminum wiring film 65 and the source region and the drain region 57 in the memory cell region, and the aluminum wiring film 65 and the source region and the region 59 in the peripheral region 59 are connected electrically by way of the contact hole 66. Then, a predetermined patterning is applied to the aluminum wiring film 65 to form a structure shown in Fig. 34.

[0029]

As shown in Fig. 35, a smooth coat film 67 is formed above the entire main surface of the silicon substrate 1. A through hole 70 is formed in the smooth coat film 67. Then, an aluminum wiring film 69 is formed on the smooth coat film 67. The aluminum wiring film 69 and the aluminum wiring film 65 are connected electrically by way of the through hole 70. As shown in Fig. 36, a predetermined patterning is applied to the aluminum wiring film 69. As described above, the existent step for the method of manufacturing a flash memory is thus completed.

[0030]

As shown in Fig. 31 and Fig. 32, a stacked structure comprising the HTO film 35, the silicon nitride film 37, and the HTO film 42 is formed between the control gate 51 and the floating gate 49. This stacked structure is called ONO film. The following three characteristics are required for the films formed between the floating gate 49 and the control gate 51.

[0031]

① They have good insulative property between the control gate 51 and the floating gate 49.

[0032]

② They are resistant to leakage. That is, electric charges accumulated in the floating gate 49 are kept from leakage.

[0033]

③ They have high specific dielectric constant. The reason ③ is as described below. In order to accumulate a great amount of electric charges in the floating gate 49, it is necessary to increase the voltage for the floating gate 49 when the charges are supplied from the floating gate 49. Accordingly, it is preferred that the voltage for the floating gate 49 is also near the voltage for the control gate 51 when a voltage is applied to the control gate 51. For this purpose, it is preferred that the specific dielectric constant of the film between the floating gate 49 and the control gate 51 is higher.

[0034]

While the HTO film is excellent for ① and ② above, it is poor for ③. On the contrary, while the silicon nitride film is excellent for ③, it is poor for ①, ②. The ONO film adopts both the advantage of the HTO film and the advantage of the silicon nitride film.

[0035]

By the way, the HTO film 42 as the uppermost film of the

ONO film is referred to as Top Oxide which is preferably as thick as possible in order to prevent current leakage. This is disclosed also in 1990 IEEE/IRPS pp 145 - 149 A MODEL FOREPROM INTRINSIC CHARGE LOSS THROUGH OXIDE-NITRIDE-OXIDE (ONO) INTERPOLY DIELECTRIC. The HTO film 35 as the lowest film of the ONO film is referred to as Bottom Oxide.

[0036]

[Subject to be Solved by the Invention]

As described above, it is preferred that the thickness of the ONO film between the control gate 51 and the floating gate 49 is as thick as possible for preventing peak current, whereas it is preferred that the film is as thin as possible to increase the static capacity in order to decrease the potential difference between the control gate 51 and floating gate 49. Accordingly, it is necessary that the thickness of the ONO film is within a predetermined optimum range.

[0037]

However, in the existent method described above, since the silicon oxide films 39, 41 as the gate insulative film in the peripheral region are formed after the formation of the ONO film, there was large error for the thickness of the HTO film 42 as the uppermost layer of the ONO film due to various factors to be described below. Therefore, the static capacity between the control gate 51 and the floating gate 49 varies and the extent of the initial distribution of the threshold voltage V_{th} increases between the transistors to bring about a problem of

deteriorating the operation characteristics of the flash memory. Fig. 38 shows the initial V_{th} distribution between the transistors due to the factors other than the distribution for the film thickness of the uppermost HTO film (shown by arrow A in the graph) and the initial HTO distribution between transistors in a case where scattering is caused for the thickness of the HTO film as the uppermost layer of the existent step described above (shown by arrow B) in comparison. According to the graph of Fig. 38, it can be seen that the extent of the V_{th} distribution caused by scattering of the HTO film 42 is innegligibly large.

[0038]

The relation of the static capacity between the control gate 51 and the floating gate 49, to the threshold voltage of the memory cell transistor can be represented according to the following equation by referring to Fig. 39.

[0039]

[Equation 1]

$$V_{thCG} = \frac{C_{cf} + (C_{fa} + C_{fb} + C_{fs})}{C_{fa} + C_{fb} + C_{fs}} V_{thFG}$$

V_{thCG} : threshold voltage of the memory cell transistor in a case of applying a voltage to the control gate

$C_{cf} \approx C_{fa} + C_{fb} + C_{fs}$

[0040]

The above-described equation C_{ef} is further expressed by the following equation.

[0041]

[Equation 2]

$$C_{ef} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}$$

C_1 = capacity of HTO film 35

C_2 = capacity of silicon nitride film 37

C_3 = capacity of HTO film 42

[0042]

C_3 in the equation described above is in a reverse proportion with the thickness of the HTO film 42. The reason why the thickness of the HTO films 42 varies in a case of forming the silicon nitride film 39, 41 in the peripheral region after forming the ONO film in the existent step described above can be explained as below with reference to the following Table 1.

[0043]

[Table 1]

(unit: Å)

	Thickness of HTO film 42 as the uppermost layer of ONO film	Thickness of gate insulative film (silicon oxide film 39) of high voltage withstanding	Thickness of gate insulative film (silicon oxide film 41) of 5 V type transistor

		transistor	
Deposition of HTO film (220 Å)	+ 220 ± 22		
Gate oxidation (first: 290 Å)	hydrofluoric acid treatment: -60 ± 6	thermal oxidation + 290 ± 29	
Gate oxidation (second : 150Å)	hydrofluoric acid treatment: -60 ± 6	hydrofluoric acid treatment: - 30 ± 3 increment due to second gate oxidation: 40 ± 4	+150 ± 15
Film thickness total	100 ± 34	300 ± 36	150 ± 15

[0044]

At first, in the step shown in Fig. 25, when the HTO film 42 as the uppermost layer of the ONO film is formed, since the error for the thickness of the HTO film deposition by the CVD method is about ± 10%, the thickness for the deposited HTO film is 220 ± 22 Å. (+) in Table 1 indicates the direction of increasing the thickness, while (-) indicates the direction of decreasing the thickness. In the subsequent first gate oxidation step shown in Figs. 26 and 27, RCA cleaning is at first applied over the entire surface of the silicon substrate 1. The RCA cleaning is a semiconductor wet cleaning method proposed by Mr. Werner Kern of RCA Co in USA in 1970 and, specifically, removal of particles on the wafer surface, etc. is conducted by using a liquid chemical in which ammonia, aqueous hydrogen peroxide (H_2O_2) and water are mainly mixed at a predetermined ratio.

[0045]

Then, for removing unnecessary spontaneous oxide films,

etc. on the surface of the silicon substrate 1, after applying etching with a 50:1 aqueous HF solution (volumic ratio between water and HF of 50:1) for about 30 sec, that is, so-called fluoric acid treatment, thermal oxidation is conducted. In the hydrofluoric acid treatment, the HTO film 42 is removed by about 60 Å by etching as can be seen from the graph shown in Fig. 37. Since the error in the etching amount of the hydrofluoric acid treatment is also about ± 10%, the change for the film thickness of the HTO film 42 is -60 ± 6 Å. In this case, the thickness for both of the silicon oxide films 39, 41 is increased by the thermal oxidation for the silicon substrate to about 290 Å and, thus, the thickness of the silicon oxide film as the gate insulative film in the high voltage withstanding transistor is 290 ± 19 Å while considering that the error for the thickness of the thermal oxide film formed by thermal oxidation is ± 10%. For the silicon oxide film 41 as the gate insulative film of 5 V type transistor, since this is removed by etching after the first gate oxidation, Table 1 indicates that the silicon oxide film 41 is not formed by the first gate oxidation.

[0046]

Then, by the second gate oxidation, the silicon oxide film 41 of the 5 V type transistor is formed to a thickness of about 150 Å and, at the same time, the thickness for the silicon oxide film 39 of the high voltage withstanding transistor also increases to a thickness of about 300 Å. In this case, the silicon oxide film 39 is removed by about 30 Å by the

hydrofluoric acid treatment applied before the thermal oxidation step for gate oxidation as can be seen from the graph shown in Fig. 37. Further, the HTO film 42 is removed by about 60 Å during this hydrofluoric acid treatment. Considering ± 10% error for the etching amount due to the hydrofluoric acid treatment, ± 10% error for the thickness of the silicon oxide film formed by thermal oxidation and ± 10% error for the deposition amount of the HTO film by CVD, scattering as shown in the lowest column in Table 1 is caused to the thickness of the HTO film 42, the silicon oxide film 39 and the silicon oxide film 41.

[0047]

The reason why the thickness of the silicon oxide film 39 formed to the thickness of about 290 Å in the first gate oxidation step increases to about 30 Å thickness by way of the second gate oxidation step after removal of the thickness of about 30 Å by the hydrofluoric treatment can be explained as below, referring to the graph in Fig. 40.

[0048]

The thermal oxidation time t and the oxide film thickness x_0 are generally represented in accordance with the square rule of the oxidation as:

$$x_0^2 = \beta t,$$

which form a parabolic graph as shown in Fig. 40. In the equation above, β is a constant which can be experimentally determined easily. For example, in a case where the constant β

is set so as to agree with the graph shown in Fig. 40, the thickness of the silicon oxide film 39 is about 260 Å just after the hydrofluoric acid treatment as the pretreatment in the second gate oxidation film, and this corresponds to the point B in the graph shown in Fig. 40. In the next second gate oxidation step, the silicon oxide film 39 transfers from the point B in Fig. 40 to the point C after about 2.25 min, during formation of the silicon oxide film 41 to the thickness of about 150 Å, that is, during transfer from the original point to the point A in Fig 40 by thermal oxidation for about 2.25 min. Accordingly, the thickness of the silicon film 39 at that instance (point C in Fig. 40) is about 300 Å.

[0049]

As has been described above, since large scattering is caused for the film thickness of the HTO film 42 in the prior art step described above, the static capacity between the control gate 51 and the floating gate 49 varied and, as a result, this brought about a problem that the extension of the threshold voltage distribution between the transistor was increased.

[0050]

In view of the foregoing problems in the prior art, it is an object of the manufacturing method for a nonvolatile semiconductor memory device according to the present invention to facilitate control for the film thickness of the dielectric film between the control gate and the floating gate thereby improving the accuracy of distribution of the threshold voltage

between the memory cells.

[0051]

[Means for the Solution of the Subject]

The method of manufacturing a nonvolatile semiconductor device according to the present invention concerns a method of manufacturing a nonvolatile semiconductor memory device having a memory cell region and a peripheral circuit region. The manufacturing method includes a step of forming an insulative film over the main surface of a semiconductor substrate, a step of forming a floating gate on the insulative film, a step of forming a dielectric film formed by stacking a first silicon oxide film, a silicon nitride film and a second silicon oxide film successively over the floating gate, and a step of forming a control gate on the dielectric film. The characteristic feature of the invention resides in that the step of forming the dielectric film includes a step of successively forming a first silicon oxide film and a silicon nitride film and a step of forming a second silicon oxide film on the silicon nitride film after passing the gate oxidation step at least for once.

[0052]

[Function]

According to the manufacturing step of the invention, since a gate oxidation step for forming the gate insulative film of transistors in the peripheral circuit region is included at least for once before forming the silicon oxidation film as the uppermost layer of the dielectric film between the control gate

and the floating gate, this decreases the thermal oxidation step after forming the silicon oxidation film as the uppermost layer of the dielectric film. As a result, removal of the silicon oxide film relevant to the hydrofluoric acid treatment as the pretreatment to the thermal oxidation step for gate oxidation can be minimized. Since the number of steps for the etching amount of the silicon oxide film by the hydrofluoric treatment is decreased, scattering for the thickness of the silicon oxide film as the uppermost layer of the dielectric film can be suppressed and, as a result, scattering of the electrostatic capacity between the control gate and the floating gate due to the scattering for the thickness of the dielectric film is suppressed. As a result, extension of distribution of the threshold voltage between the memory cell transistors can be suppressed.

[0053]

[Example]

An example for the method of manufacturing a nonvolatile semiconductor memory device according to the present invention is to be described with reference to the drawings. Constituent elements identical with or corresponding to those in the prior art are to be explained while using identical reference numerals.

[0054]

At first, in the same manner as in the prior art described above, after the steps shown in Fig. 16 to Fig. 24, an HTO film 35 of about 100 Å thickness is formed above the entire

surface of a silicon substrate 1 by a CVD method. Then, a silicon nitride film 37 of about 100 Å thickness is formed also by the CVD method (Fig. 1).

[0055]

Then, a memory cell region and a p-well region 13 are covered with a resist film 13, boron ions are implanted in the n-well region 11 to control the threshold voltage of the transistor to be formed over the n-well region 11 (refer to Fig. 2). Then, the memory cell region and the n-well region 11 are covered with a resist film 104, boron ions are implanted to the p-well region 13 in the peripheral region to control the threshold voltage of the transistor to be formed over the p-well region 13 (Fig. 3).

[0056]

As shown in Fig. 4, only the memory cell region is covered with a resist film 105, and the silicon substrate 1 is etched for the peripheral region to remove the silicon oxide film 29 on the surface of the n-well region 11 and the p-well region 13. Then, spontaneous oxide films and other impurities over the surface of the silicon substrate 1 in the peripheral region are removed by a hydrofluoric acid treatment of applying 50:1 HF etching for about 30 sec. Then, thermal oxidation is applied to form a silicon oxide film 41a of about 220 Å thickness on the surface of the n-well 11 and the p-well 13 in the peripheral region, and a silicon oxide film 39a also of about 220 Å on the surface of the n-well 111 and the p-well 113,

to obtain a structure shown in Fig. 5.

[0057]

Then, as shown in Fig. 6, the memory cell region and the n-well 111 and the p-well 113 to form a high voltage withstanding transistor are covered with a resist film 106, and the surface of the n-well 11 and the p-well 13 to form a 5 V type transistor are etched to remove the silicon oxide film 41a.

[0058]

Then, after conducting RCA cleaning and, further, conducting a hydrofluoric acid treatment by applying 50:1 HF etching for about 30 sec, thermal oxidation is applied again to form a silicon oxide film 41b of about 50 Å thickness on the surface of the n-well 11 and p-well 13. In this step, since the surface of the n-well 111 and the p-well 113 is also thermally oxidized, the thickness of the silicon oxide film 39a is increased as shown in Fig. 7 to a thickness of about 200 Å.

[0059]

Then, as shown in Fig. 8, a high temperature oxide film is deposited above the entire surface of the silicon substrate 1 by a CVD method, and an HTO film 42 of about 100 Å thickness is formed on the surface of the silicon nitride film 37 in the memory cell region. At the same time, a silicon oxide film 41c of about 100 Å thickness is formed on the n-well 11 and the p-well 13 in the peripheral region, and a silicon oxide film 39b also of about 100 Å thickness is formed on the n-well 111 and the p-well 113. As a result, a so-called ONO film which is a

dielectric film formed by stacking the HTO film 35, the silicon nitride film 37 and the HTO film 42 is formed. A silicon oxide film 41 as a gate insulative film comprising silicon oxide films 41b, 41c is formed over a region in which the 5 V-type transistor is formed. Further, a silicon oxide film 39 as a gate insulative film comprising silicon oxide films 39a, 39b is formed over the region in which the high withstanding voltage transistor is formed.

[0060]

Subsequently, by way of the same steps as those of the prior art steps described above shown in Fig. 29 to Fig. 36, a nonvolatile semiconductor memory device is completed.

[0061]

The film thickness for the HTO film 42, the silicon oxide film 39 and the silicon oxide film 41 in this example is as shown in the following Table 2 while considering the ± 10% error for the etching amount by a hydrofluoric acid treatment conducted as a pretreatment to the gate oxidation step, ± 10% error for the thickness of the thermal oxide film in the gate oxidation step, and ± 10% error for the film thickness in the deposition of the HTO film.

[0062]

[Table 2]

(unit: Å)

	Thickness of HTO film 42 as the uppermost layer of ONO film	Thickness of gate insulative film (silicon oxide film 39) of high voltage withstanding transistor	Thickness of gate insulative film (silicon oxide film 41) of 5 V type transistor
Gate oxidation (first: 220 Å)		+ 220 ± 22	
Gate oxidation (second: 50 Å)		hydrofluoric acid treatment: - 30 ± 3 increment due to second gate oxidation: 10 ± 1	+50 ± 5
Deposition of HTO film (100 Å)	+100 ± 10	+100 ± 10	+100 ± 10
Film thickness total	100 ± 10	300 ± 36	150 ± 15

[0063]

As can be seen from numeral values shown in Table 2, when compared with Table 1 for the prior art described above, error for the thickness of the HTO film 42 is restricted extremely without increasing the error for the thickness of the silicon oxide film 39 and the silicon oxide film 41 not so much. Accordingly, scattering of the thickness of the HTO film 42 as the uppermost layer of the ONO film between the memory cell transistors is decreased and as a result, the scattering for the thickness of the ONO film can also be restricted. Accordingly, scattering of the static capacity between the control gate 51 and the floating gate 49 can be suppressed to decrease the extent of the distribution of the threshold voltage between the

transistors.

[0064]

Then, a method of manufacturing a nonvolatile semiconductor memory device in other embodiment of the invention is to be described with reference to Fig. 9 to Fig. 11.

[0065]

The manufacturing steps in this embodiment are identical with the embodiment described previously up to the steps in Fig. 5 of the previous embodiment which is the first gate oxidation film. However, in this embodiment, the aimed value for the thickness of the thermal oxide film formed by the first gate oxidation is defined as about 160 Å. Then, in this embodiment, a high temperature oxide film, that is, an HTO film is deposited to about 160 Å above the entire surface of the silicon substrate 1 by a CVD method as shown in Fig. 9. In Fig. 9, (a) shows a memory cell region on the right and a 5 V type transistor forming region on the left, while (b) shows a region for forming the high voltage withstanding transistor in the peripheral region. The thus formed HTO film constitutes an HTO film 42 as the uppermost layer of the ONO film in the memory cell region and constitutes a silicon oxide film 41d in a region for forming the 5 V type transistor and, further, constitutes a silicon oxide film 39c for the high voltage withstanding voltage type transistor.

[0066]

Then, as shown in Fig. 10, the memory cell region and the

high voltage withstanding transistor forming region are covered with a resist film 107 and the silicon oxide films 41d, 41a in the 5 V type transistor forming region are removed by etching to expose the surface of the n-well 11 and the p-well 13.

[0067]

Then, the second gate oxidation is conducted. In this gate oxidation step, after at first conducting the fluoric acid treatment as a pretreatment to the gate oxidation step (etching with an aqueous solution of 50:1 HF for 30 sec), thermal oxidation is conducted so as to form a thermal oxide film of about 150 Å thickness. As a result, as shown in Fig. 11, a silicon oxide film 41 as a thermal oxide film at a thickness of about 150 Å is formed above the surface of the silicon substrate 1 in the 5 V type transistor forming region, which constitutes the gate oxide film of the 5 V type transistor. Further, also the thickness of the silicon oxide film 39a as the thermal oxide film above the surface of the silicon substrate 1 in the high voltage withstanding transistor forming region is increase in the gate oxidation step, and a silicon oxide film 39 as a gate insulative film of the high voltage withstanding transistor at a thickness of about 300 Å is constituted together with the silicon oxide film 39.

[0068]

Change of the film thickness in the HTO film 42, the silicon oxide film 39 and the silicon oxide film 41 is shown in the following Table 3 while taking the error for the film

thickness formed in each of the steps in this embodiment into consideration.

[0069]

[Table 3]

(unit: Å)

	Thickness of HTO film 42 as the uppermost layer of ONO film	Thickness of gate insulative film (silicon oxide film 39) of high voltage withstanding transistor	Thickness of gate insulative film (silicon oxide film 41) of 5 V type transistor
Gate oxidation (first: 160 Å)		160 ± 16	
Deposition of HTO film (220 Å)	160 ± 16	160 ± 16	
Gate oxidation (second : 150Å)	hydrofluoric acid treatment: -60 ± 6	hydrofluoric acid treatment: - 60 ± 12 increment due to second gate oxidation: 40 ± 4	thermal oxidation 150 ± 15
Film thickness total	100 ± 22	300 ± 42	150 ± 15

[0070]

As apparent from the result of Table 3, according to this embodiment, the scattering of the film thickness for the HTO film 42 can be suppressed without increasing the scattering for the film thickness of the silicon oxide film 39 and the silicon oxide film 41.

[0071]

Further, according to this embodiment, since the silicon oxide film 41 as the gate insulation film for the 5 V type transistor is formed only with the thermal oxide film by the

gate oxidation step, the film quality as the gate insulative film is improved somewhat compared with the case of a stacked structure comprising the HTO film and the thermal oxide film as in the embodiment described above.

[0072]

[Effect of the Invention]

As has been described above, according to the present invention, the scattering for the thickness of the HTO film as the uppermost layer of the ONO film can be suppressed without increasing the scattering of the thickness for the gate oxide film of the transistor formed in the peripheral circuit region. As a result, scattering of the electrostatic capacity between the control gate and the floating gate can be suppressed to decrease the extension of the threshold voltage distribution of the memory cell transistor to improve the characteristics as the nonvolatile semiconductor memory device.

[Brief Description of the Drawings]

[Fig. 1] is a fragmentary cross sectional view of a silicon substrate showing a first step of an embodiment for the manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 2] is a fragmentary cross sectional view of a silicon substrate showing a second step of an embodiment for the manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 3] is a fragmentary cross sectional view of a silicon substrate showing a third step of an embodiment for the manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 4] is a fragmentary cross sectional view of a silicon substrate showing a fourth step of an embodiment for the manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 5] is a fragmentary cross sectional view of a silicon substrate showing a fifth step of an embodiment for the manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 6] is a fragmentary cross sectional view of a silicon substrate showing a sixth step of an embodiment for the manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 7] is a fragmentary cross sectional view of a silicon substrate showing a seventh step of an embodiment for the manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 8] is a fragmentary cross sectional view of a silicon substrate showing an eighth step of an embodiment for the manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 9] is a fragmentary cross sectional view of a silicon substrate showing a first step of another embodiment of

a manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 10] is a fragmentary cross sectional view of a silicon substrate showing a second step of another embodiment of a manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 11] is a fragmentary cross sectional view of a silicon substrate showing a third step of another embodiment of a manufacturing method of a nonvolatile semiconductor memory device in accordance with the present invention.

[Fig. 12] is a block diagram showing a general constitution of a flash memory.

[Fig. 13] is an equivalent circuit diagram showing a schematic constitution of a memory matrix shown in Fig. 12.

[Fig. 14] is a fragmentary cross sectional view showing a cross sectional structure of one memory transistor constituting a flash memory.

[Fig. 15] (a) is a schematic plan view showing a planar arrangement of an existent stack gate type flash memory, (b) is a fragmentary cross sectional view taken along line A-A in (a).

[Fig. 16] is a fragmentary cross sectional view of a silicon substrate showing a first step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 17] is a fragmentary cross sectional view of a silicon substrate showing a second step of an embodiment of an

existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 18] is a fragmentary cross sectional view of a silicon substrate showing a third step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 19] is a fragmentary cross sectional view of a silicon substrate showing a fourth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 20] is a fragmentary cross sectional view of a silicon substrate showing a fifth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 21] is a fragmentary cross sectional view of a silicon substrate showing a sixth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 22] is a fragmentary cross sectional view of a silicon substrate showing a seventh step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 23] is a fragmentary cross sectional view of a silicon substrate showing an eighth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 24] is a fragmentary cross sectional view for a silicon substrate taken along line B-B in Fig. 20.

[Fig. 25] is a fragmentary cross sectional view of a silicon substrate showing a ninth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 26] is a fragmentary cross sectional view of a silicon substrate showing a tenth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 27] is a fragmentary cross sectional view of a silicon substrate showing an eleventh step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 28] is a fragmentary cross sectional view of a silicon substrate showing a twelfth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 29] is a fragmentary cross sectional view of a silicon substrate showing a thirteenth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 30] is a fragmentary cross sectional view of a silicon substrate showing a fourteenth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 31] is a fragmentary cross sectional view of a silicon substrate showing a fifteenth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 32] is a fragmentary cross sectional view for a silicon substrate taken along line C-C in Fig. 31.

[Fig. 33] is a fragmentary cross sectional view of a silicon substrate showing a sixteenth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 34] is a fragmentary cross sectional view of a silicon substrate showing a seventeenth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 35] is a fragmentary cross sectional view of a silicon substrate showing an eighteenth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 36] is a fragmentary cross sectional view of a silicon substrate showing a nineteenth step of an embodiment of an existent manufacturing method of a nonvolatile semiconductor memory device.

[Fig. 37] is a graph showing the etching characteristics of a CVD oxide film and a thermal oxide film with 50:1 HF aqueous solution in comparison.

[Fig. 38] is a graph showing the voltage distribution of

threshold values between the memory cell transistors in a normalized state in a case caused by factors excluding the thickness distribution of the HTO film as an uppermost layer of an ONO film (arrow A in the graph) and in a case including the factors described above (arrow B in the graph).

[Fig. 39] is an explanatory view symbolizing the static capacity in each of the portions of the memory cell.

[Fig. 40] is a graph showing the time for thermal oxidation and the thickness of the oxide film formed by thermal oxidation.

[Description for References]

1	silicon substrate
29	silicon oxide film
31	polycrystal silicon film
35	HTO film
37	silicon nitride film
43	polycrystal silicon film

る。

【図３０】従来の不揮発性半導体記憶装置の製造方法の一例の第１４工程を示すシリコン基板の部分断面図である。

【図３１】従来の不揮発性半導体記憶装置の製造方法の一例の第１５工程を示すシリコン基板の部分断面図である。

【図３２】図３１のＣ－Ｃ線に沿うシリコン基板の部分断面図である。

【図３３】従来の不揮発性半導体記憶装置の製造方法の一例の第１６工程を示すシリコン基板の部分断面図である。

【図３４】従来の不揮発性半導体記憶装置の製造方法の一例の第１７工程を示すシリコン基板の部分断面図である。

【図３５】従来の不揮発性半導体記憶装置の製造方法の一例の第１８工程を示すシリコン基板の部分断面図である。

【図３６】従来の不揮発性半導体記憶装置の製造方法の一例の第１９工程を示すシリコン基板の部分断面図である。

【図３７】５０：１ＨＦ水溶液による、ＣＶＤ酸化膜と熱酸化膜とのエッチング特性を対比して示す図である。

【図３８】ＯＮＯ膜最上層のＨＴＯ膜の膜厚分布を除く要因による場合（図の矢印Ａ）と、その要因を含む場合（図の矢印Ｂ）のメモリセルトランジスタ間のしきい値電圧分布を正規化して示す図である。

【図３９】メモリセルの各部の静電容量を記号化するための説明図である。

【図４０】熱酸化時間と、その熱酸化により形成される酸化膜の膜厚との関係を示す図である。

【符号の説明】

１　シリコン基板

２９　シリコン酸化膜

３１　多結晶シリコン膜

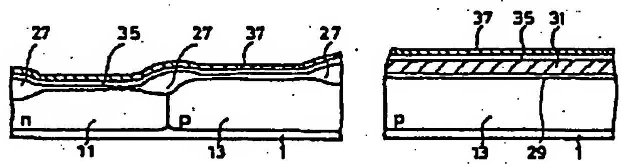
３５　ＨＴＯ膜

３７　シリコン窒化膜

４３　多結晶シリコン膜

Fig. 1 【図１】

Peripheral region　Memory cell region



1: silicon substrate

11: n-well

13: p-well

27: field oxide film

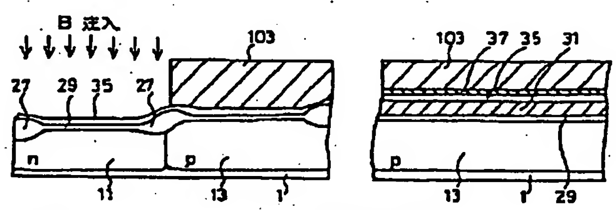
29: silicon oxide film

31: polycrystal silicon film

35: HTO film

37: silicon nitride film

B implanted 【図２】 Fig. 2

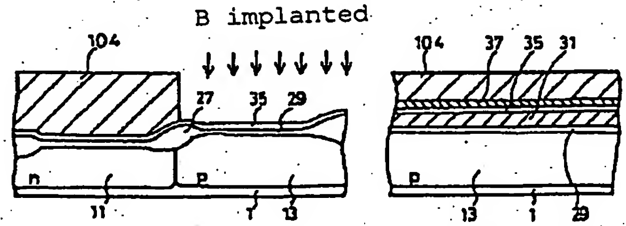


103: レジスト膜

103: resist film

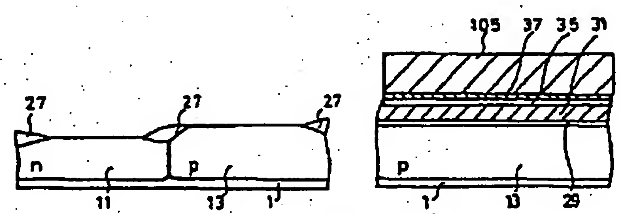
Fig. 3 【図３】

B implanted



104: resist film

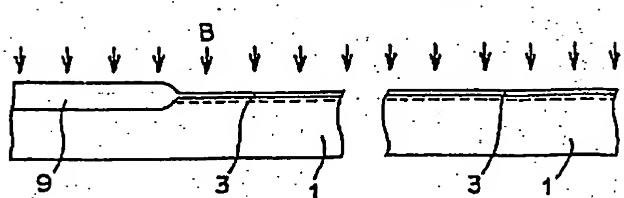
【図４】 Fig. 4



105: レジスト膜

105: resist film

【図１７】 Fig. 17



【図１８】 FIg. 18

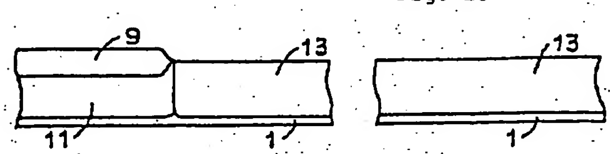
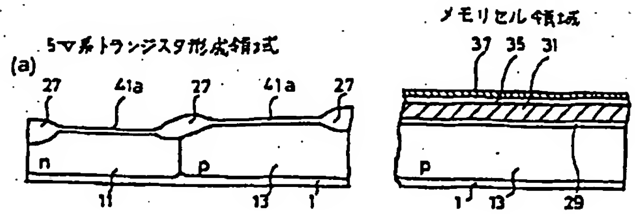


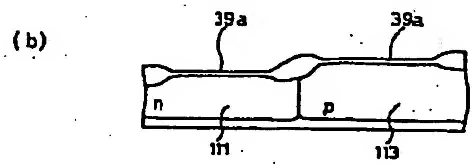
Fig. 5

(a) 5 V type transistor forming region

Memory cell region

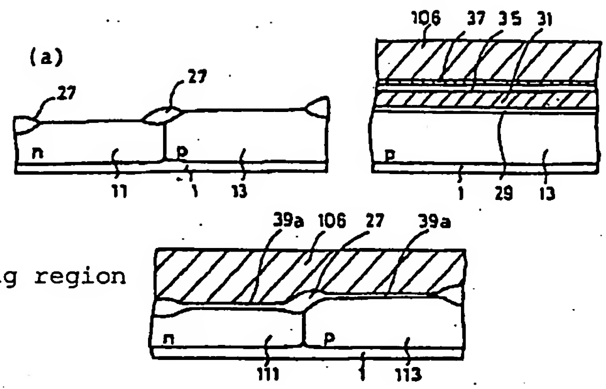


(b) High voltage withstanding transistor forming region

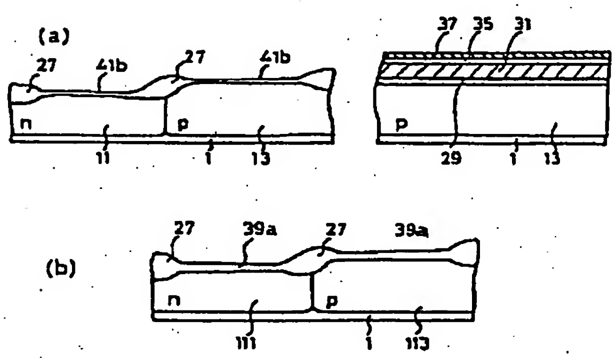


111: nウェル　111 n-well
113: pウェル　113 p-well

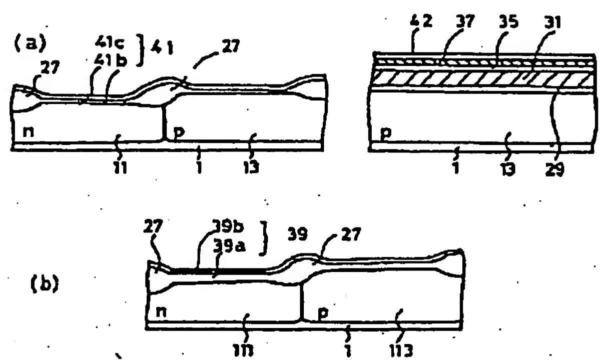
【図6】 Fig. 6



【図7】 Fig. 7

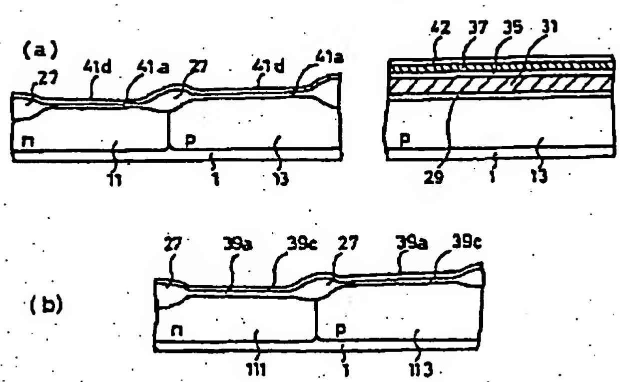


【図8】 Fig. 8



39, 41: シリコン酸化膜　39 41 siliconnoxide film
42: HTO膜　42 HTO film

【図9】 Fig. 9



【図10】 Fig. 10

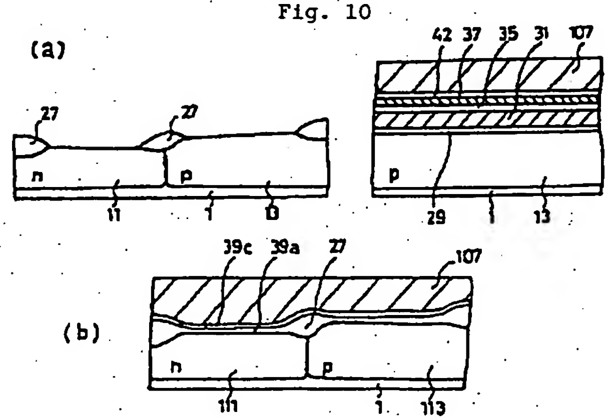
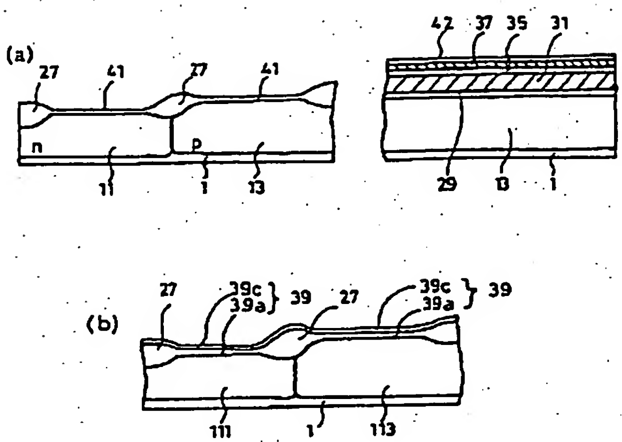
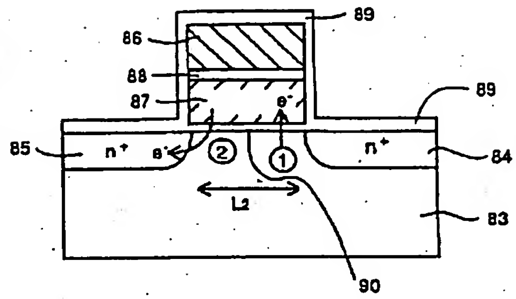


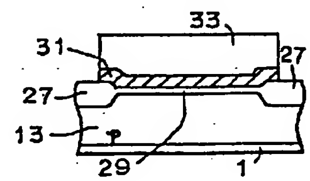
Fig. 11　【図11】



【図14】 Fig. 14



【図24】 Fig. 24



【図12】
Fig. 12

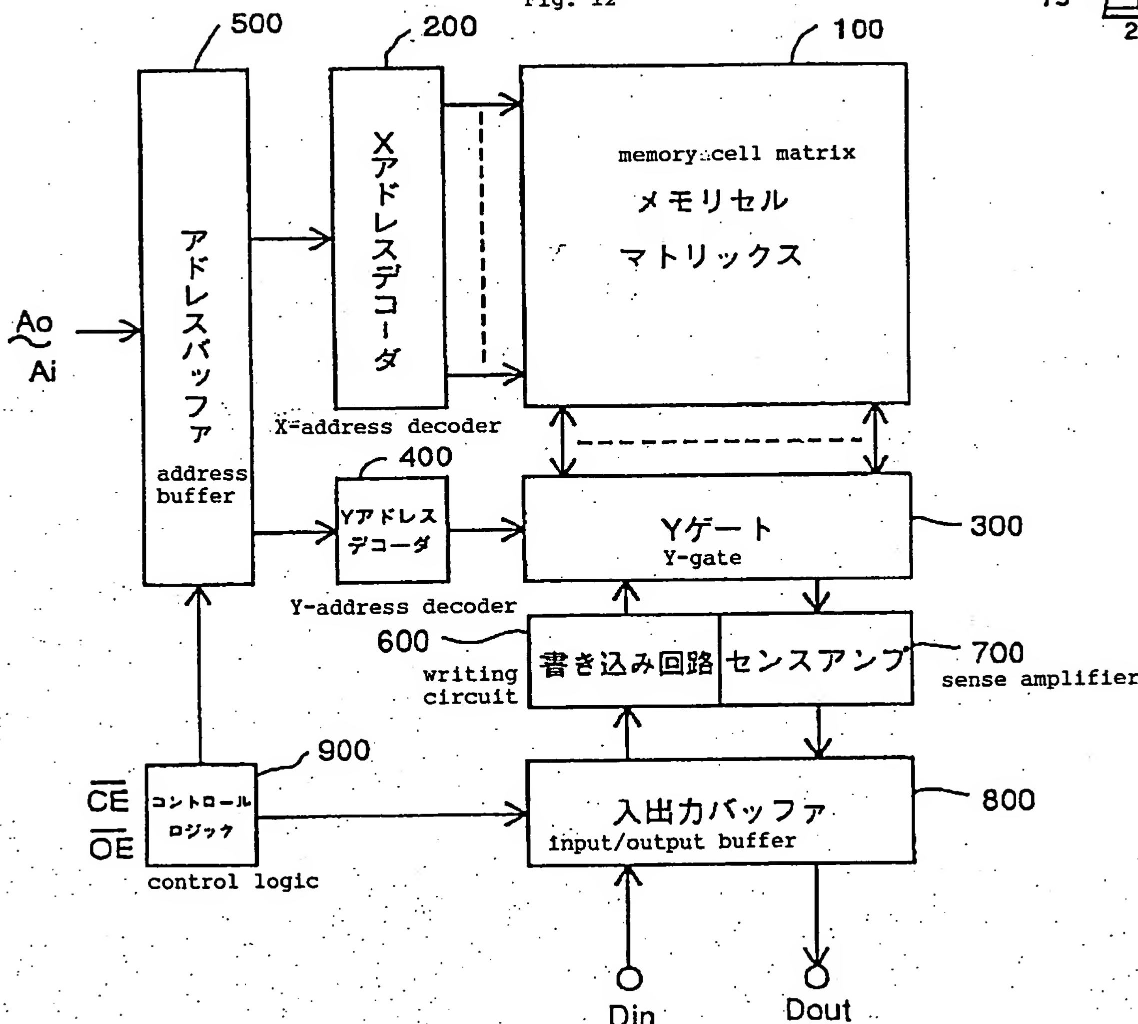


Fig. 13 【図13】

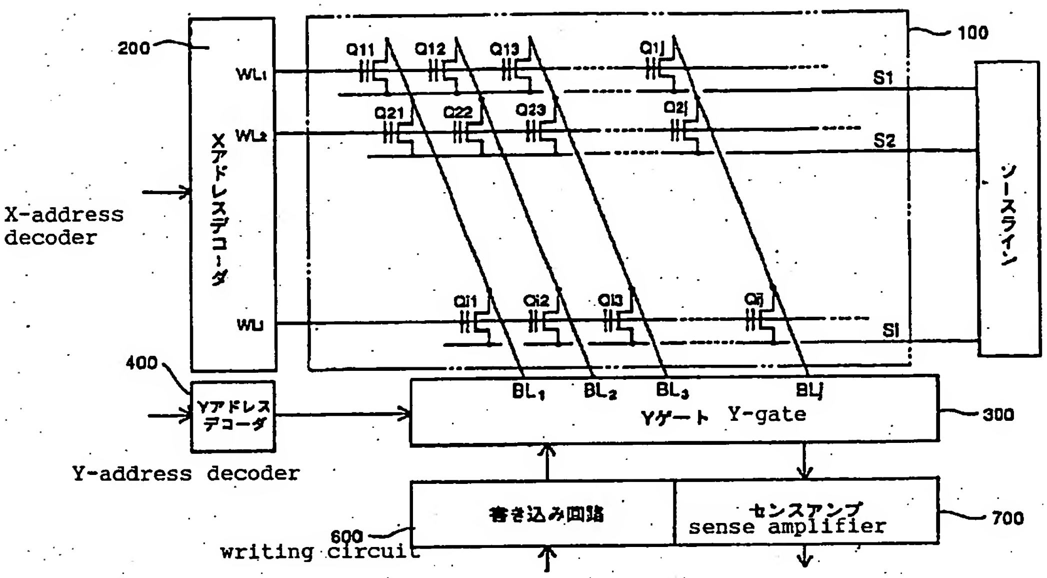
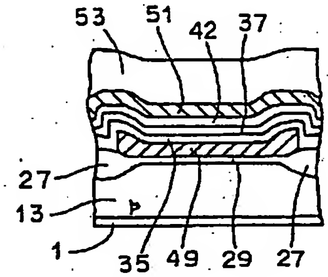
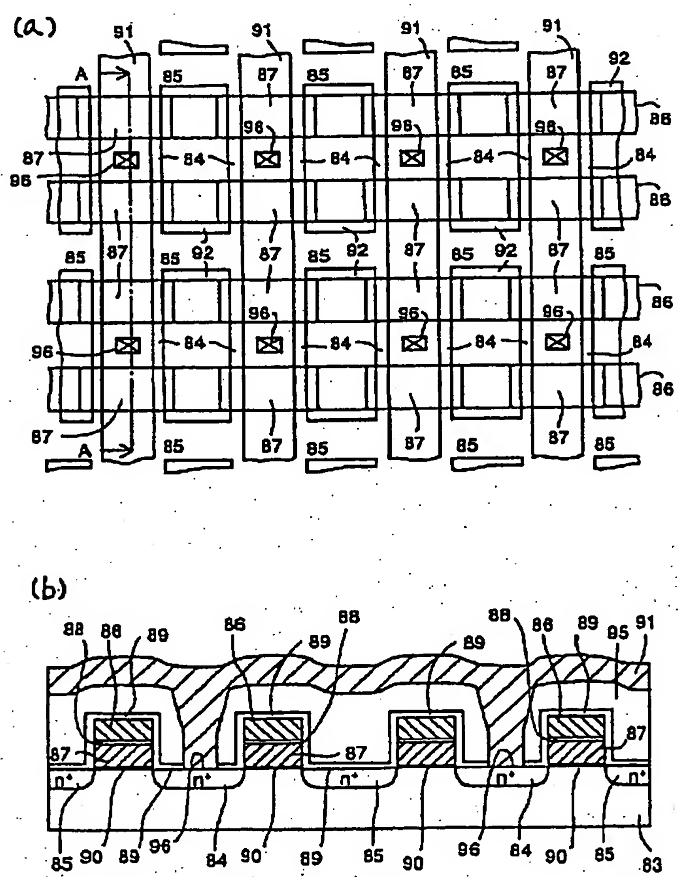


Fig. 32 【図32】

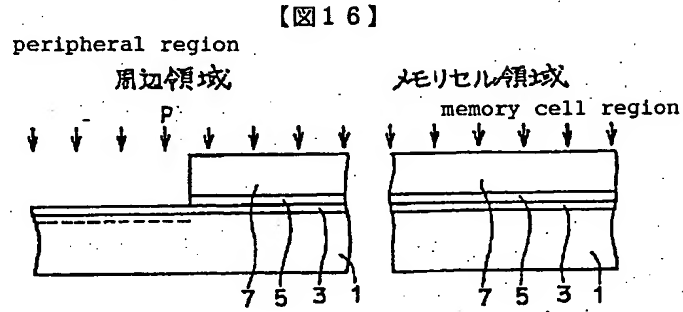


source line

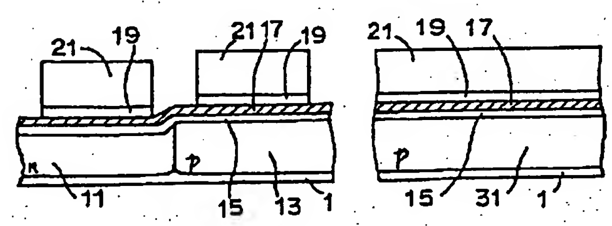
【図15】



【図16】



【図19】 Fig. 19



【図20】 Fig. 20

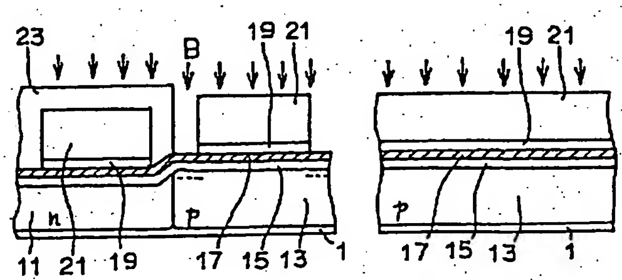


Fig. 21 【図２１】

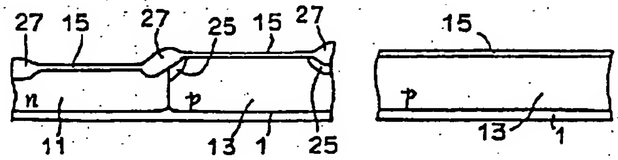


Fig. 22 【図２２】

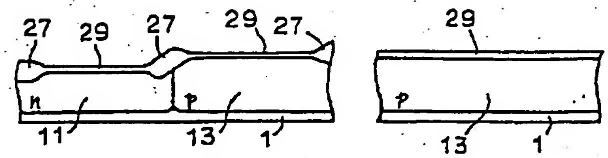


Fig. 23 【図２３】

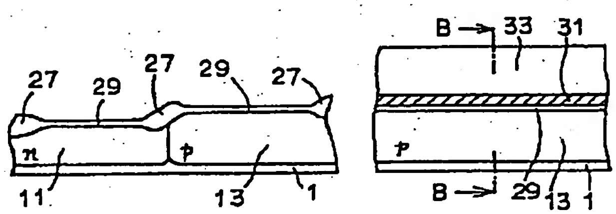


Fig. 25 【図２５】

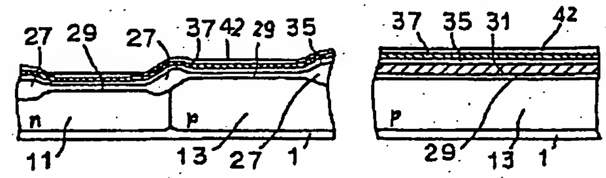
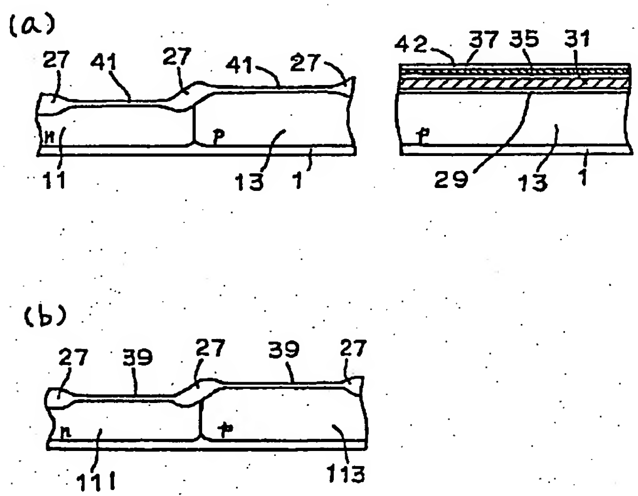
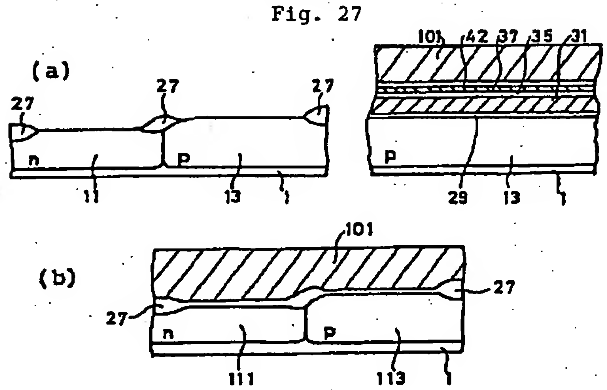


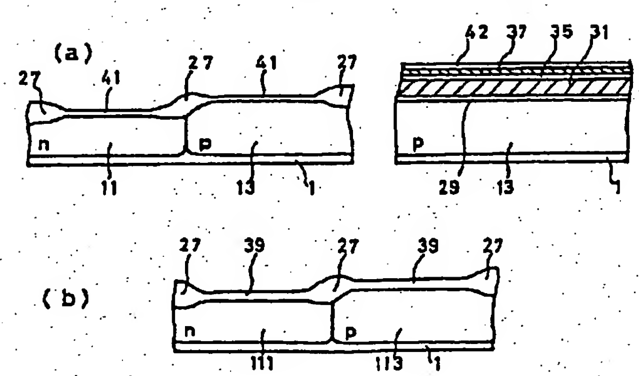
Fig. 26 【図２６】



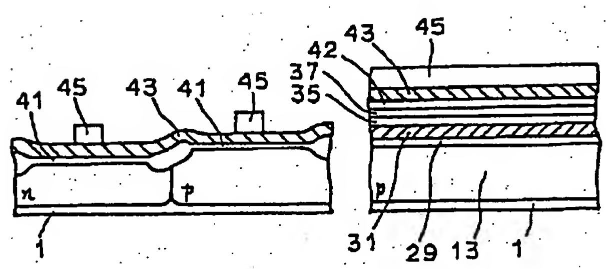
【図２７】
Fig. 27



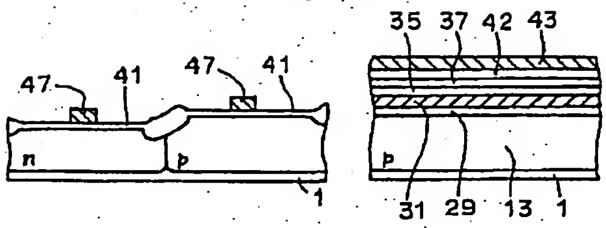
【図２８】 Fig. 28



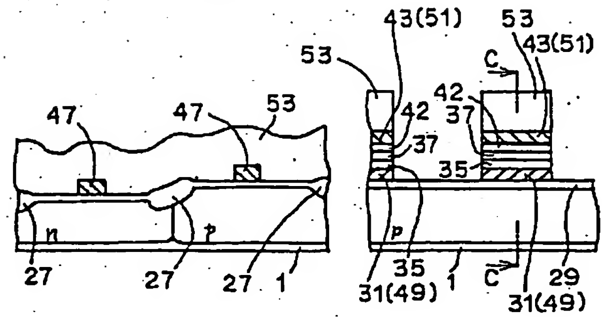
【図２９】 Fig. 29



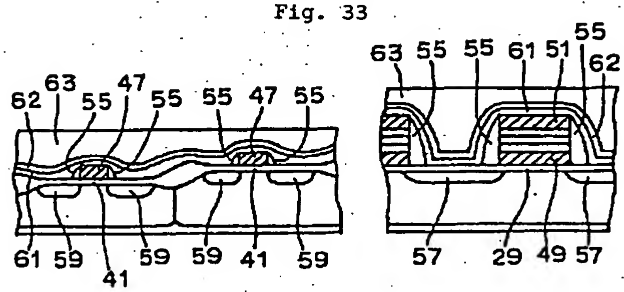
【図30】
Fig. 30



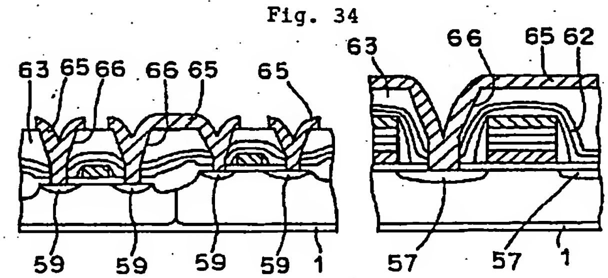
【図31】
Fig. 31



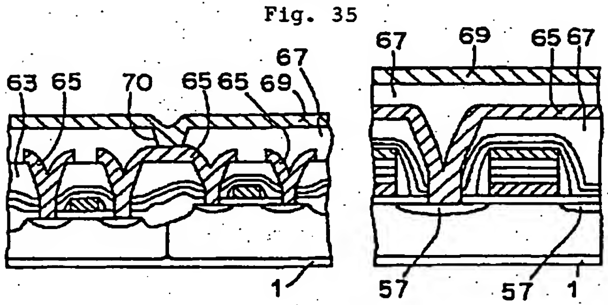
【図33】
Fig. 33



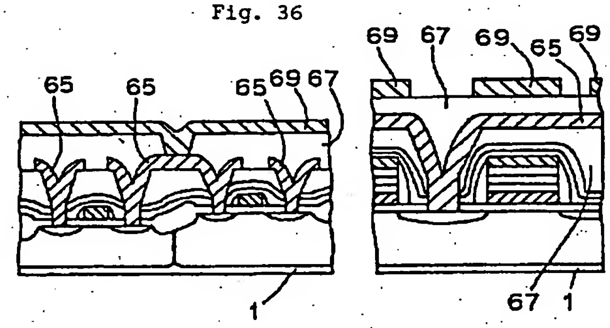
【図34】
Fig. 34



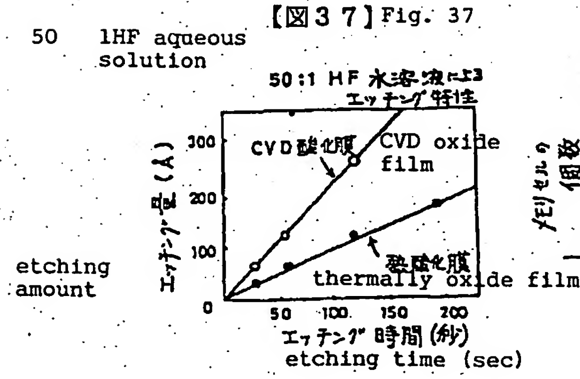
【図35】
Fig. 35



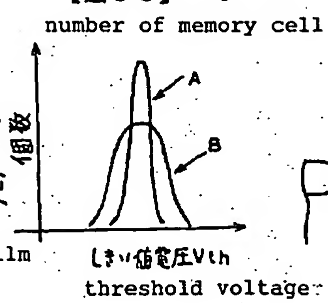
【図36】
Fig. 36



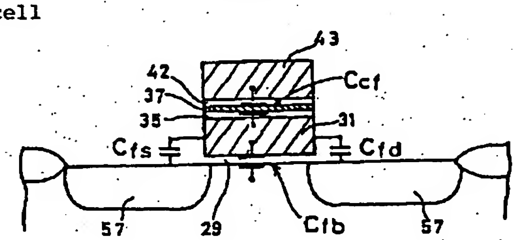
【図37】Fig. 37



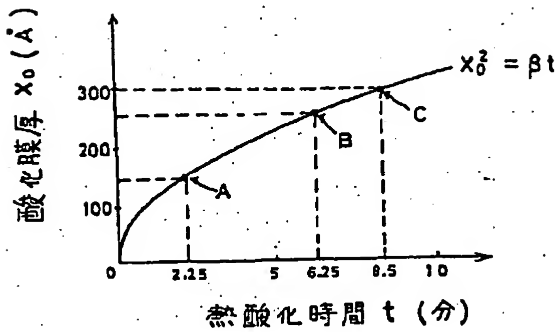
【図38】 Fig. 38



【図39】 Fig. 39



【図40】 Fig. 40



oxide film thickness

thermal oxidation time t (min)